IN THE CLAIMS

1 (Currently Amended). A method comprising:

storing data at a first density in a first cell in a first memory array;

storing data at a second density in a second cell in the first memory array; and

dynamically changing the number of bits stored per cell in the course of writing to the memory.

2 (Original). The method of claim 1 wherein storing data at a second density in a second cell includes storing fewer bits per cell in one of said first or second cells.

3 (Previously Presented). The method of claim 1 including changing the number of bits stored per cell dynamically.

4 (Original). The method of claim 2 including storing data at levels which are spaced from one another in said cell in order to improve the read fidelity.

5 (Original). The method of claim 4 including storing data in a cell including a plurality of levels and filling less than all of said levels.

6 (Original). The method of claim 5 including storing data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.

7 (Currently Amended). An article comprising a medium storing instructions, that, if executed, enable a processor-based system to:

store data at a first density in a first cell in a first memory;

store data at a second density in a second cell in said first memory array; and

dynamically change the number of bits stored per cell in the course of writing to the memory.

8 (Original). The article of claim 7 further storing instructions that enable the processor-based system to store fewer bits per cell in one of said first or second cells.

9 (Canceled).

10 (Original). The article of claim 8 further storing instructions that enable the processor-based system to store data at levels which are spaced from one another in said cell in order to improve the read fidelity.

11 (Original). The article of claim 10 further storing instructions that enable the processor-based system to store data in a cell including a plurality of levels and fill less than all of said levels.

12 (Original). The article of claim 11 further storing instructions that enable the processor-based system to store data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.

13 (Currently Amended). A memory comprising:

a memory array including a first and second cell; and

a controller coupled to said array to store data in said array at a first density in the first cell and to store data at a second density in the second cell wherein said controller to dynamically change the number of bits stored per cell in the course of writing to the memory.

14 (Original). The memory of claim 13 wherein said memory is a flash memory.

15 (Original). The memory of claim 14 wherein said memory is a multi-level cell memory.

16 (Original). The memory of claim 13 wherein said controller stores fewer bits per cell in one of said first or second cells.

Claim 17 (Canceled).

18 (Previously Presented). The memory of claim 13 wherein said controller stores data at levels that are spaced from one another in said cell in order to improve the read fidelity.

19 (Original). The memory of claim 18 wherein said controller stores data in a cell including a plurality of levels and fills less than all of the levels.

20 (Original). The memory of claim 13 wherein said controller stores data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.